REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated June 4, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-15 are under consideration in this application. Claims 1, 5, 9 and 11 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention. New claims 13-15 are being added to recite other embodiments described in the specification.

Additional Amendments

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-8 were rejected under 35 U.S.C. § 103(a) as being unpatenable over US Pat. No. 5,091,784 to Someya et al. (hereinafter "Someya")in view of US Pat. No. 6,144,355 Murata et al. (hereinafter "Murata"). Kubota et al. (6,437,768) was cited as being pertinent to the present application. This rejection has been carefully considered, but is most respectfully traversed.

The liquid crystal display device of the invention (Embodiment 1 in Fig. 2 and Embodiment 2 in Fig. 23), as now recited in claim 1, having a liquid crystal display panel 100, a plurality of cascade-connected liquid crystal drive circuits 130, 140 (Fig. 1) for sequentially transferring a signal (Fig. 1; page 1, third line to the bottom; ""the display data and clock signal

as sent out of the timing controller will be delivered and passed between respective drain drivers in a one-by-one manner," page 3, lines 17-19), and a plurality of signal lines (Fig. 1, not numbered) formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the drive circuits. Each of the drive circuits comprises: an image input terminal connected with one of the signal lines to receive an image signal being input thereto; a clock input terminal connected with another one of the signal lines to receive an external clock signal being input thereto; a clock compensation circuit 200 (e.g. a phase-locked loop in Fig. 3, page 17, 2nd and 3rd paragraph) for generating an internal clock signal CLL2 based on the external clock signal CL2i thereby compensating for a duty ratio deviation of the external clock signal CL2i (page 3, last paragraph; page 4, lines 20-23; page 6, line 9; page 15, 4th paragraph; page 50, 4th paragraph), said internal clock signal CLL2 swinging from a first voltage to a second voltage lower than the first voltage; a data storage circuit CST for storing therein the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal CLL2 (Fig. 12; page 24, line 18 to page 25, line 5); a data bus for transmitting the image signal from the data storage circuit; a voltage select circuit for selecting from the image signal on the data bus a voltage used to drive the liquid crystal display panel and then outputting the voltage selected; and a clock signal output circuit 134 for outputting the internal clock signal (i.e., the compensated external clock data) as a subsequent external clock signal CL2o ("*A display data latch clock signal as will be output to the outside [a subsequent cascade-connected drain driver] from the drain driver 130 is indicated by "CL2o.*" page 15, 3rd paragraph; Fig. 2) to a subsequent liquid crystal drive circuit.

The duty ratio deviation of the external clock signal is caused by at least one of an internal characteristic of the respective drive circuit, such as the threshold voltage (Vth) of each MOS transistor in a CMOS inverter circuit, a factor on the signal lines, or repeated signal transferring events (page 5, last paragraph to page 6, first paragraph). Preferably, the internal clock signal (i.e., the compensated external clock signal) generated by the clock compensation circuit has a duty ratio of 50% ("Output Clock Signal" in Figs. 4, 9; page 18, lines 21-24; "Clock Signal (inverted)" in Fig. 26).

As the clock signal duty ratio variation increases via the increase of drive circuit stages, it will finally become impossible to accept any display data at the later driver circuits. The

present invention avoid the problem by compensating the duty ratio of each external clock signal form one drive circuit to a subsequent drive circuit.

The invention (Embodiment 3 in Figs. 24-25), as now recited in claim 5, is also directed to a liquid crystal display device having a liquid crystal display element 52, a plurality of cascade-connected liquid crystal drive circuits, and a plurality of signal lines formed over an edge portion of the liquid crystal display element for transmitting a signal between any two of the drive circuits. Each of the liquid crystal drive circuits comprises: a data input terminal connected with one of the signal lines to receive an image signal being input thereto; a clock compensation circuit for inputting an external clock signal and outputting an internal clock signal, the internal clock signal having a first period for outputting a first voltage and a second period for outputting a second voltage; a data latch circuit for taking thereto the image signal at a timing of a voltage change from the first voltage to the second voltage or at a timing of a voltage change from the second voltage to the first voltage of the internal clock signal; a data bus for transmitting the image signal from the data latch circuit; a voltage output circuit for outputting a voltage selected from the image signal on the data bus to the liquid crystal display element; a data output circuit for outputting the image signal on the data bus to a subsequent liquid crystal drive circuit; a clock circuit being operable to correct a duty ratio deviation of the external clock signal to provide the internal clock signal; and a clock signal output circuit for outputting the internal clock signal as a subsequent external clock signal to a subsequent liquid crystal drive circuit.

Applicants respectfully contend that neither Someya nor any other cited prior art reference teaches or suggests "a plurality of cascade-connected liquid crystal drive circuits for sequentially transferring a signal connected by a plurality of signal lines, each drive circuit 130 having a clock compensation circuit 200 for generating an internal clock based on the external clock signal (inputted form a preceding drive circuit) by compensating for a duty ratio deviation of the external clock signal caused by an internal characteristic of the respective drive circuit 130 and/or a factor on the signal lines, **then outputting the internal clock signal as a subsequent external clock signal to a subsequent liquid crystal drive circuit**" as the invention. The plurality of signal lines are formed over an edge portion of the liquid crystal display panel, and the image signal is stored each time a change of the internal clock signal (from a second voltage to a first voltage or vise verse) occurs.

As presented in the prior response and implicitly admitted by the Examiner, Someya is silent regarding *compensating* for a duty ratio deviation of the external clock signal in one drive circuit caused by an internal characteristic of the respective drive circuit or a factor on the signal lines between the cascade-connected drive circuits, then outputting the compensated/corrected external clock signal to a subsequent drive circuit. The control circuit 7 in Someya comprises a clock generator 8, and different output clocks are generated by the generator. Someya does not teach a plurality of signal lines formed over an edge portion of the liquid crystal display panel for transmitting a signal between any two of the of cascade-connected drive circuits.

The clock compensation circuit 34 (i.e., a PLL circuit) in Murata is relied upon by the Examiner to teach the clock compensation circuit 200 of the invention. However, the horizontal clock signal CK1 is input via one or a plurality of PLL circuits 34 (Figs. 4-6) to each shift register section 26 ***in parallel*** (rather than to "one clock controller in one drive circuit than another clock controller of the subsequent cascade-connected drive circuit") ***in series.*** Accordingly, the PLL circuits 34 only correct "*distortion of waveform of the horizontal clock signal CK1 and deviation or "breakage" of the duty ratio [due to adverse influence with the time constant as defined by inherent parasitic or stary capacitances on wiring lines (col. 7, lines 42-44)] thereof*", but not to correct any deviation of the external clock signal caused by an internal characteristic of the respective drive circuit 130. Murata fails to teach any output circuit for transmitting the internal clock signal, i.e., the compensated/corrected external clock signal, to a subsequent liquid crystal drive circuit. Neither does Murata teach the external clock signal is compensated/corrected in order to transmit the compensated/corrected signal to the subsequent liquid crystal drive circuit.

Applicants contend that neither Someya nor Murata teaches or discloses each and every feature of the present invention as disclosed in at least independent claims 1 and 5. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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September 2, 2003

SPF/JCM/JT